PATENT ABSTRACTS OF JAPAN

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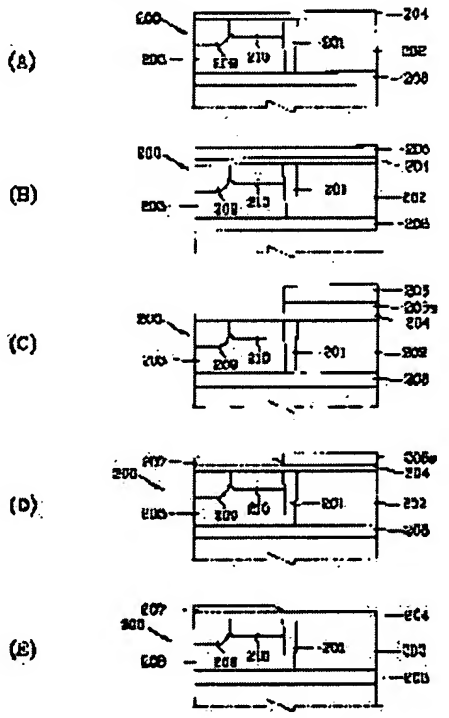
(54) METHOD OF FORMING GATE INSULATING FILM FOR SEMICONDUCTOR ELEMENT

(57)Abstract:
PROBLEM TO BE SOLVED: To provide a method of forming gate insulating film for semiconductor element by which the thicknesses of gate insulating films can be adjusted in accordance with the characteristics of each element in a semiconductor substrate and, at the same time, the substrate can be prevented from being damaged.
SOLUTION: In this method, a first gate insulating film 204 is formed on a semiconductor substrate 200 and a silicon nitride film 205 and a photoresist film are successively formed on the insulating film 204. Then a photoresist pattern 206 is formed by leaving the photoresist on a low-voltage element forming area 202 in a photolithography step. In addition, a silicon nitride film pattern 205a is formed by using the photoresist pattern 206 as a mask and the pattern 206 is removed. Finally, a second gate insulating film 207 is formed only on a high-voltage element forming area 203 by using the silicon nitride film pattern 205a as an oxidation preventing mask pattern and the pattern 205a is removed.



LEGAL STATUS

[Date of request for examination]

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CLAIMS

[Claim(s)]
[Claim 1] The process which forms the 1st gate dielectric film in the whole top face of the semi-conductor substrate which has the 1st and the 2nd-element formation field which were separated by the component isolation region, The process which forms an antioxidizing mask pattern only in said 1st Guesde insulator layer top face of said 1st-element formation field, The gate-dielectric-film formation approach of the semiconductor device characterized by having the process which forms the 2nd gate dielectric film in said 1st gate-dielectric-film top face of said 2nd-element formation field, and the process which removes said antioxidizing mask pattern by using said antioxidizing mask pattern as a mask.
[Claim 2] It is the gate-dielectric-film formation approach of the semiconductor device according to claim 1 characterized by being a field for said 1st-element formation field being a field for forming a low-battery component, and for said 2nd-element formation field forming a high-tension component.
[Claim 3] Said 1st gate dielectric film and 2nd gate dielectric film are the gate-dielectric-film formation approach of the semiconductor device according to claim 1 or 2 characterized by forming by the oxidizing [thermally] method.
[Claim 4] Said antioxidizing mask pattern is the gate-dielectric-film formation approach of the semiconductor device any one publication of claim 1-3 characterized by being a silicon nitride.
[Claim 5] The gate-dielectric-film formation approach of the semiconductor device any one publication of claim 1-4 characterized by applying in order to form the gate dielectric film of the component of the smart integrated circuit which accumulated two or more components in which a component property carries out difference.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the gate-dielectric-film formation approach of the semiconductor device in which the electrical characteristics accumulated on one semi-conductor substrate carry out difference about the gate-dielectric-film formation approach of a semiconductor device.
[0002]
[Description of the Prior Art] the smart integrated circuit which generally combined the control function and the actuation function in one chip -- the output section -- about 15 -- it constitutes from a high-tension (high power) transistor (a high-tension component is called hereafter) which operates by the high tension of -80V -- having -- the logic section -- about 5 -- it consists of usual transistors (a low-battery component is called hereafter) which operate by V or less low battery.
[0003] Such a smart integrated circuit is mainly used for actuation, such as a display like a liquid crystal display (Liquid Crystal Display;LCD), and HDTV (High Definition TV). And structure and the manufacture approach carry out difference of said high-tension component and the low-battery component, and the thickness of those gate dielectric film carries out difference especially. That is, since high tension is impressed to a gate electrode in the case of a high-tension component, when gate dielectric film is thin, there is a possibility that it may be destroyed. Then, according to the applied voltage concerned, it is necessary to form the gate dielectric film of a high-tension component more thickly than the gate dielectric film of a low-battery component so that high applied voltage can also be borne.
[0004] For example, in the usual smart integrated circuit, the gate dielectric film of a low-battery component is formed in the thickness of about 200A to generally the gate dielectric film of a high-tension component being formed in the thickness of about 400A. For this reason, the gate dielectric film of a high-tension component and the gate dielectric film of a low-battery component cannot be formed simultaneously. Thus, the manufacture approach of the gate dielectric film of the conventional smart integrated circuit device constituted is explained, referring to drawing 2 (A) - (C). In addition, drawing 2 is drawing having shown the structure of the conventional smart integrated circuit device roughly, and does not show actual structure and a actual dimension.
[0005] First, as shown in drawing 2 (A), the semi-conductor substrate 100 110, i.e., 1st about 300A gate dielectric film which consists of diacid-ized silicon oxide formed in the whole top face of a wafer by the oxidizing [thermally] method, is formed. The semi-conductor substrate 100 has high-tension component formation field 100a classified by component isolation region 100c, and low-battery component formation field 100b, as shown in drawing 2 (A). 100d of insulator layers is formed in the predetermined depth of said semi-conductor substrate 100, and the function which raises an isolation property is done so in it. And the impurity wells 101 and 102 are formed in said high-tension component formation field 100a.
[0006] Subsequently, as shown in drawing 2 (B), after forming the photoresist film pattern 111 in the top face of high-tension component formation field 100a and component isolation region 100c, the 1st gate dielectric film 110 of the top face of said low-battery component formation field 100b is removed using the wet etching method. Furthermore, the photoresist film pattern 111 of the top face of said high-tension component formation field 100a and component isolation region 100c is removed.
[0007] Then, the 1st gate dielectric film 110 on said high-tension component formation field 100a and component isolation region 100c and the 2nd gate dielectric film 112 which gives the oxidizing [thermally] method to the whole top face of low-battery component formation field 100b, and consists of diacid-ized silicon oxide are formed. In this way, as shown in drawing 2 (C), manufacture of the gate dielectric film of the conventional smart integrated circuit device is completed.

[0008] In spite of crossing said 2nd gate dielectric film 112 to a component top face and forming it at the same process, it serves as thickness which is formed in the thickness of about 100A and is different on each field, for example to being formed in the thickness of about 200A on the top face of high-tension component formation field 100a on the top face of low-battery component formation field 100b. As a result, 1st about 300A gate dielectric film 110 and 2nd about 100A gate dielectric film 112 are formed in the top face of high-tension component formation field 100a, and it is about 400A. The gate dielectric film of thickness is formed. Thus, the reason formed is because the growth rate of the 2nd gate dielectric film 112 corresponding to high-tension component formation field 100a becomes slow by controlling oxidation of the semi-conductor substrate with which the 1st insulator layer 110 formed on said high-tension component formation field 100a consists of silicon.
[0009] As shown in drawing 2 (C), if manufacture of gate dielectric film is completed, manufactures of a high-tension component and a low-battery component, such as formation of a gate electrode, will be performed on the top face of this gate dielectric film, but since it separates from the meaning of this invention, explanation is omitted.
[0010]
[Problem(s) to be Solved by the Invention] it be alike , and it be the process in which give the wet etching method and the 1st gate dielectric film of the top face of a low battery component formation field be remove after [appropriate] forming the 1st gate dielectric film in the gate dielectric film formation approach of such a conventional smart integrated circuit device , the breakage on the top face of a semi-conductor substrate used as the active field of a low battery component occurred , and there be an inconvenient point that the property of a component fell .
[0011] Moreover, in the formation process of the 2nd gate dielectric film, where the 1st gate dielectric film is formed in the top face of a high-tension component formation field, in order to form the 2nd gate dielectric film, there was an inconvenient point of being hard to adjust the thickness of the gate dielectric film of a high-tension component formation field. Then, this invention was made in view of such a conventional trouble, and the object can prevent breakage on the semi-conductor substrate part used as the active field in the 1st-element formation field, and is to offer the gate-dielectric-film formation approach of a semiconductor device that the thickness of gate dielectric film can be adjusted easily.
[0012]
[Means for Solving the Problem] For this reason, the process which forms the 1st gate dielectric film in the whole top face of the semi-conductor substrate with which invention concerning claim 1 has the 1st and the 2nd-element formation field which were separated by the component isolation region, The process which forms an antioxidizing mask pattern only in said 1st Guesde insulator layer top face of said 1st-element formation field, It was characterized by having the process which forms the 2nd gate dielectric film in said 1st gate-dielectric-film top face of said 2nd-element formation field, and the process which removes said antioxidizing mask pattern by using said antioxidizing mask pattern as a mask.
[0013] Moreover, invention concerning claim 2 is a field for said 1st-element formation field to form a low-battery component, and said 2nd-element formation field was characterized by being a field for forming a high-tension component. Moreover, invention concerning claim 3 was characterized by forming said 1st gate dielectric film and 2nd gate dielectric film by the oxidizing [thermally] method.
[0014] Moreover, invention concerning claim 4 was characterized by said antioxidizing mask pattern being a silicon nitride. Moreover, invention concerning claim 5 was characterized by applying in order to form the gate dielectric film of the component of the smart integrated circuit which accumulated two or more components in which a component property carries out difference.
[0015]
[Embodiment of the Invention] Hereafter, the gestalt of operation of this invention is explained using a drawing. One operation gestalt which applied the gate-dielectric-film formation approach of the semiconductor device concerning this invention to the smart integrated circuit is explained below, referring to drawing 1 (A) - (E). As shown in drawing 1 (A), the semi-conductor substrate 200 is equipped with the low-battery component formation field 202 as a 1st-element formation field classified in the component isolation region 201, and the high-tension component formation field 203 as a 2nd-element formation field as usual. Moreover, an insulator layer 208 is formed in the predetermined depth of the semi-conductor substrate 200. Furthermore, the impurity wells 209 and 210 are formed in the high-tension component formation field 203.
[0016] Next, the oxidizing [thermally] method is given to the top face of said semi-conductor substrate 200, and the 1st gate dielectric film 204 is formed in it at the thickness of about 200A. In this case, as for said 1st gate dielectric film 204, it is desirable to form by silicon oxide by the oxidizing [thermally] method. Next, as shown in drawing 1 (B), the silicon nitride 205 is formed in the top face of said 1st gate dielectric film 204.

[0017] Next, after forming the photoresist film in the top face of said silicon nitride 205, as a photolithography process is given and it was shown in drawing 1 (C), it leaves the photoresist film only to the top face of the low-battery component formation field 202, and the photoresist pattern 206 is formed, the silicon nitride 205 of said high-tension component formation field 203 top face is selectively removed by using said photoresist pattern 206 as a mask, and silicon nitride pattern 205a is formed. Then, as said photoresist pattern 206 is removed and it was shown in drawing 1 (D), the 2nd gate dielectric film 207 is formed only in the top face of the 1st gate dielectric film 204 on said high-tension component formation field 203 by using said silicon nitride pattern 205a as an antioxidizing mask pattern. As for said 2nd gate dielectric film 207, at this time, it is desirable to give the oxidizing [thermally] method and to form a diacid-ized silicone film. If it does in this way, only in consideration of the property of a high-tension component, the 2nd gate dielectric film 207 can be formed in sufficient thickness by said silicon nitride pattern 205a, without taking into consideration component property change of a low-battery component, since oxidation of the 1st gate dielectric film 204 of the top face of the low-battery component formation field 202 is prevented.
[0018] Namely, what is necessary is to add further the 2nd gate dielectric film 207 which is 200A, and just to form it, since 200A is already formed with the 1st gate dielectric film 204 when the whole gate-dielectric-film thickness on said high-tension component formation field 203 is 400A. Finally, the wet etching method is given, said silicon nitride pattern 205a is removed, and as shown in drawing 1 (E), the gate-dielectric-film formation process of a semiconductor device is completed.
[0019] In addition, although this operation gestalt showed the gate-dielectric-film formation approach of the semiconductor device at the time of applying to a smart integrated circuit, an application circuit should just be a circuit which accumulated two or more semiconductor devices in which not only this but electrical characteristics carry out difference on one semi-conductor substrate.
[0020]
[Effect of the Invention] Since the thickness of each gate dielectric film of the 1st and the 2nd-element formation field accumulated into one chip can be adjusted according to each component property according to this invention as explained above, the dependability of a semiconductor device can be improved. Furthermore, since it is not necessary to etch gate dielectric film like before and becomes possible to prevent breakage on a semi-conductor substrate front face, the dependability of a semiconductor device can be improved.

[Translation done.]

TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the gate-dielectric-film formation approach of the semiconductor device in which the electrical characteristics accumulated on one semi-conductor substrate carry out difference about the gate-dielectric-film formation approach of a semiconductor device.

[Translation done.]

PRIOR ART

[Description of the Prior Art] the smart integrated circuit which generally combined the control function and the actuation function in one chip -- the output section -- about 15 -- it constitutes from a high-tension (high power) transistor (a high-tension component is called hereafter) which operates by the high tension of -80V -- having -- the logic section -- about 5 -- it consists of usual transistors (a low-battery component is called hereafter) which operate by V or less low battery.
[0003] Such a smart integrated circuit is mainly used for actuation, such as a display like a liquid crystal display (Liquid Crystal Display;LCD), and HDTV (High Definition TV). And structure and the manufacture approach carry out difference of said high-tension component and the low-battery component, and the thickness of those gate dielectric film carries out difference especially. That is, since high tension is impressed to a gate electrode in the case of a high-tension component, when gate dielectric film is thin, there is a possibility that it may be destroyed. Then, according to the applied voltage concerned, it is necessary to form the gate dielectric film of a high-tension component more thickly than the gate dielectric film of a low-battery component so that high applied voltage can also be borne.
[0004] For example, in the usual smart integrated circuit, the gate dielectric film of a low-battery component is formed in the thickness of about 200A to generally the gate dielectric film of a high-tension component being formed in the thickness of about 400A. For this reason, the gate dielectric film of a high-tension component and the gate dielectric film of a low-battery component cannot be formed simultaneously. Thus, the manufacture approach of the gate dielectric film of the conventional smart integrated circuit device constituted is explained, referring to drawing 2 (A) - (C). In addition, drawing 2 is drawing having shown the structure of the conventional smart integrated circuit device roughly, and does not show actual structure and a actual dimension.
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[Translation done.]

EFFECT OF THE INVENTION

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[Translation done.]

TECHNICAL PROBLEM

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[Translation done.]

MEANS

[Means for Solving the Problem] For this reason, the process which forms the 1st gate dielectric film in the whole top face of the semi-conductor substrate with which invention concerning claim 1 has the 1st and the 2nd-element formation field which were separated by the component isolation region, The process which forms an antioxidizing mask pattern only in said 1st Guesde insulator layer top face of said 1st-element formation field, It was characterized by having the process which forms the 2nd gate dielectric film in said 1st gate-dielectric-film top face of said 2nd-element formation field, and the process which removes said antioxidizing mask pattern by using said antioxidizing mask pattern as a mask.
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[0017] Next, after forming the photoresist film in the top face of said silicon nitride 205, as a photolithography process is given and it was shown in drawing 1 (C), it leaves the photoresist film only to the top face of the low-battery component formation field 202, and the photoresist pattern 206 is formed, the silicon nitride 205 of said high-tension component formation field 203 top face is selectively removed by using said photoresist pattern 206 as a mask, and silicon nitride pattern 205a is formed. Then, as said photoresist pattern 206 is removed and it was shown in drawing 1 (D), the 2nd gate dielectric film 207 is formed only in the top face of the 1st gate dielectric film 204 on said high-tension component formation field 203 by using said silicon nitride pattern 205a as an antioxidizing mask pattern. As for said 2nd gate dielectric film 207, at this time, it is desirable to give the oxidizing [thermally] method and to form a diacid-ized silicone film. If it does in this way, only in consideration of the property of a high-tension component, the 2nd gate dielectric film 207 can be formed in sufficient thickness by said silicon nitride pattern 205a, without taking into consideration component property change of a low-battery component, since oxidation of the 1st gate dielectric film 204 of the top face of the low-battery component formation field 202 is prevented.
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to form it, since 200A is already formed with the 1st gate dielectric film 204 when the whole gate-dielectric-film thickness on said high-tension component formation field 203 is 400A. Finally, the wet etching method is given, said silicon nitride pattern 205a is removed, and as shown in drawing 1 (E), the gate-dielectric-film formation process of a semiconductor device is completed.

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[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] Process drawing explaining 1 operation gestalt of the gate-dielectric-film formation approach of the semiconductor device by this invention
[Drawing 2] Process drawing explaining the gate-dielectric-film formation approach of the semiconductor device by the conventional technique
[Description of Notations]
200 Semi-conductor Substrate
201 Component Isolation Region
202 Low-Battery Component Formation Field
203 High-Tension Component Formation Field
204 1st Gate Dielectric Film
205 Silicon Nitride
205a Silicon nitride pattern
206 Photoresist Pattern
207 2nd Gate Dielectric Film

[Translation done.]

* NOTICES *

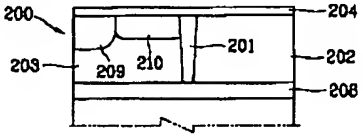
1.This document has been translated by computer. So the translation may not reflect the original precisely.

2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

(A)



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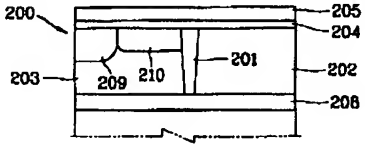

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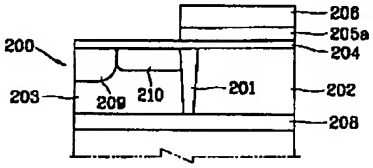

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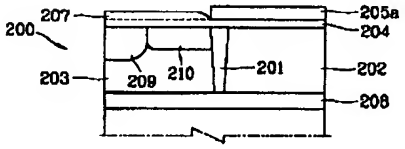

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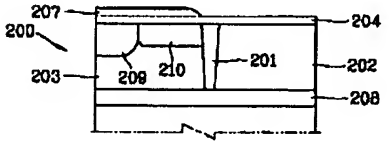
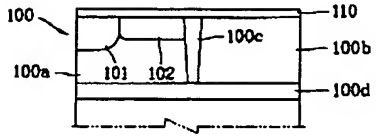


[Drawing 2]

(A)



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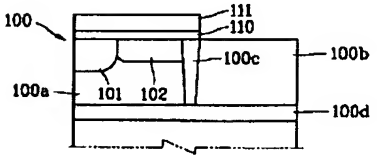

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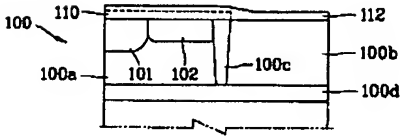

[Translation done.]